WHAT IS CLAIMED IS:

1. A memory subsystem comprising:

a memory controller configured to generate a plurality of memory requests each including address information and corresponding error detection information dependent upon said address information; and

a memory module including a plurality of memory chips for storing data, wherein said memory module is coupled to receive said plurality of memory requests;

wherein said memory module further includes an error detection circuit configured to detect an error in said address information based on said corresponding error detection information and to provide an error indication in response to detecting said error.

2. The memory subsystem as recited in claim 1, wherein each of said plurality of memory requests further include control information and said corresponding error detection information is further dependent upon said control information.

3. The memory subsystem as recited in claim 2, wherein said corresponding error detection information includes a parity bit.

4. The memory subsystem as recited in claim 2, wherein said corresponding error detection information is an error correction code.

5. The memory subsystem as recited in claim 2, wherein said error detection circuit is further configured to generate a second error detection information based upon a given received memory request and to compare said second error detection information to said corresponding error detection information to detect said error.

6. The memory subsystem as recited in claim 2, wherein if a given memory request is a memory read request, said memory controller is further configured to provide a predetermined data value in response to receiving said error indication.

7. The memory subsystem as recited in claim 2, wherein if a given memory request is a memory write request, said memory module is further configured to inhibit writing data to said plurality of memory chips in response to detecting said error.

8. The memory subsystem as recited in claim 2, wherein said memory module is further configured to provide said error indication a predetermined number of cycles after detecting said error.

9. The memory subsystem as recited in claim 8, wherein said memory controller is further configured to store a predetermined number of past memory requests in a buffer.

10. The memory subsystem as recited in claim 9, wherein said memory controller is further configured to send each of said predetermined number of past memory requests to said memory module in response to receiving said error indication.

11. The memory subsystem as recited in claim 2, wherein said memory controller is further configured to store status information in response to receiving said error indication.

12. The memory subsystem as recited in claim 11, wherein said status information includes said address information.

13. The memory subsystem as recited in claim 12, wherein said status information includes said control information.

14. The memory subsystem as recited in claim 2, wherein said memory controller is further configured to provide an interrupt to a diagnostic subsystem in response to receiving said error indication.

15. The memory subsystem as recited in claim 2, wherein said memory module is a dual in-line memory module (DIMM).

16. A computer system comprising:

a processor;

a memory subsystem coupled to said processor, said memory subsystem including:

a memory controller configured to generate a plurality of memory requests each including address information and corresponding error detection information dependent upon said address information; and

a memory module including a plurality of memory chips for storing data, wherein said memory module is coupled to receive said plurality of memory requests;

wherein said memory module further includes an error detection circuit configured to detect an error in said address information based on said corresponding error detection information and to provide an error indication in response to detecting said error.

17. The computer system as recited in claim 16, wherein each of said plurality of memory requests further include control information and said corresponding error detection information is further dependent upon said control information.

18. The computer system as recited in claim 17, wherein said corresponding error detection information includes a parity bit.

19. The computer system as recited in claim 17, wherein said corresponding error detection information is an error correction code.

20. The computer system as recited in claim 17, wherein said error detection circuit is further configured to generate a second error detection information based upon a given received memory request and to compare said second error detection information to said corresponding error detection information to detect said error.

21. The computer system as recited in claim 17, wherein if a given memory request is a memory read request, said memory controller is further configured to provide a predetermined data value in response to receiving said error indication.

22. The computer system as recited in claim 17, wherein if a given memory request is a memory write request, said memory module is further configured to inhibit writing data to said plurality of memory chips in response to detecting said error.

23. The computer system as recited in claim 17, wherein said memory module is further configured to provide said error indication a predetermined number of cycles after detecting said error.

24. The computer system as recited in claim 23, wherein said memory controller is further configured to store a predetermined number of past memory requests in a buffer.

25. The computer system as recited in claim 23, wherein said memory controller is further configured to send each of said predetermined number of past memory requests to said memory module in response to receiving said error indication.

26. The computer system as recited in claim 17, wherein said memory controller is further configured to store status information in response to receiving said error indication.

27. The computer system as recited in claim 26, wherein said status information includes said address information.

28. The computer system as recited in claim 27, wherein said status information includes said control information.

29. The computer system as recited in claim 17, wherein said memory controller is further configured to provide an interrupt to a diagnostic subsystem in response to receiving said error indication.

30. The computer system as recited in claim 17, wherein said memory module is a dual in-line memory module (DIMM).

31. A method comprising:

generating a plurality of memory requests each including address information and corresponding error detection information dependent upon said address information; and

a memory module receiving each of said plurality of memory requests;

said memory module detecting an error in said address information based on said corresponding error detection information; and

said memory module providing an error indication in response to detecting said error.

32. A memory subsystem comprising:

means for generating a plurality of memory requests each including address information and corresponding error detection information dependent upon said address information; and

a memory module coupled for receiving each of said plurality of memory requests, wherein said memory module includes:

means for detecting an error in said address information based on said corresponding error detection information; and

means for providing an error indication in response to detecting said error.

33. A memory subsystem comprising:

a memory controller configured to generate a plurality of memory requests each including control information and corresponding error detection information dependent upon said control information; and

a memory module including a plurality of memory chips for storing data, wherein said memory module is coupled to receive said plurality of memory requests;

wherein said memory module further includes an error detection circuit configured to detect an error in said control information based on said corresponding error detection information and to provide an error indication in response to detecting said error.